Analysis of Lumped Element Transistor Structures Using MRTD: The Equivalent Source Method

Robert L. Robertson and Linda P.B. Katehi

Abstract—**The Multiresolution Time Domain (MRTD) method is applied to Maxwell's equations and used to simulate lumped element transistor circuits. These lumped element circuits are expressed in terms of equivalent sources, or difference equations derived *a priori* to describe the behavior of the transistor. In this formulation, the transistor is modeled as a current source truncating the computation region. MRTD results are compared to those generated by LIBRA and good correlation is noted.**

Keywords—**MRTD, Equivalent Source method, lumped-element modeling, amplifier circuit.**

I. Introduction

THE Multiresolution Time Domain (MRTD) method is a well known technique for solving electromagnetic problems [1]. In general when applying this method to two and three dimensional microwave structures, savings in memory and execution time are shown over the conventional Finite-Difference Time Domain (FDTD) technique [1]. However, until recently [2], MRTD has not been applied to problems involving active components. Finite difference equations for the lumped element's circuit behavior are derived to produce discrete relationships between the device's terminal currents and voltages. Advantages of modeling lumped element in this way as compared to state equations is that the lumped element is easily extended across multiple FDTD cells and the need for a separate transcendental equation solver is eliminated. The inclusion of a semiconductor pn junction required by a transistor results in a set of coupled nonlinear transcendental equations that must be solved on each time step. Thus an additional procedure for solving non-linear equations must be employed such as the Newton-Raphson approach [3], [4].

It is the intent of this paper to apply MRTD to general lumped element transistor structures using the equivalent source method [5]. In comparison to the conventional FDTD method, MRTD has two advantages. First, MRTD allows for a very accurate computation of the input voltage or current terms to the lumped element circuit equations. This is primarily due to the distributed nature of the Battle-Lemarie stencil function. Second, as shown in [1], [2], the MRTD method exhibits a high degree of memory savings over conventional FDTD when applied to microwave circuits. This property is used to good advantage when simulating a structure such as a microwave transistor amplifier circuit.

II. Theoretical Formulation

As detailed in reference [5], the following equations are derived to model a transistor. Consider the lumped element equivalent circuit of the transistor shown in Figure 1, and apply Kirchoff's current law to the drain, gate and source nodes of the circuit. This results

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in the set of equations shown below:

$$I_d = I_{ds} + \dot{V}_{ds}C_{ds} - V_{gd}G_{gd} - \dot{V}_{gd}C_{gd}, \text{(1a)}$$
$$I_g = \dot{V}_{gd}C_{gd} + V_{gd}G_{gd} - V_{gs}G_{gs} - \dot{V}_{gs}C_{gs}, \text{(1b)}$$
$$I_s = -V_{gs}G_{gs} - \dot{V}_{gs}C_{gs} - I_{ds} - \dot{V}_{ds}C_{ds}. \text{(1c)}$$

Expressing the gate to drain voltage in terms of the drain to source and the gate to source voltages as follows:

$$V_{gd} \quad = \quad V_{gs} \; - \; V_{ds}. \qquad (2)$$

Now, combine equations [1] and [2] and take a time derivative of this system of equations to find the expressions for the gate to source and drain to source voltages:

$$V_{gs}^{n+1} = V_{gs}^n + \frac{\Delta}{\Psi}\Big[C_{gd}(I_d^n - I_{ds}^n) + (C_{gd} + C_{ds})I_g^n + C_{ds}G_{gd}V_{ds}^n - (C_{ds}G_{gd} + G_{gs}C_{gd} + G_{gs}C_{ds})V_{gs}^n\Big], \qquad \text{(3a)}$$

$$V_{ds}^{n+1} = V_{ds}^n + \frac{\Delta}{\Psi}\Big[(C_{gd} + C_{gs})(I_d^n - I_{ds}^n) + C_{gd}I_g^n - G_{gd}C_{gs}V_{ds}^n + (C_{gs}G_{gd} - G_{gs}C_{gd})V_{gs}^n\Big], \qquad \text{(3b)}$$

where:

$$\Psi = (C_{gd}C_{ds} \; + \; C_{gs}C_{gd} \; + \; C_{ds}C_{gs})\,. \qquad \text{(3c)}$$

The Curtice-Cubic model[6] for a general MESFET is given by introducing the following relations:

$$I_{ds} = \left(A_0 + A_1V_1 + A_2V_1^2 + A_3V_1^3\right)\tan\left(\gamma V_{ds}\right). \qquad (4)$$

The drain to source current, I_{ds}, is a cubic equation of the input voltage V_1. The coefficients A_0-A_3 are variables that are given for a specific series of transistor. The input voltage is given by the following equation:

$$V_1 \; = \; V_{gs}\Big[1 + \beta\left(V_{dso} - V_{ds}\right)\Big], \qquad (5)$$

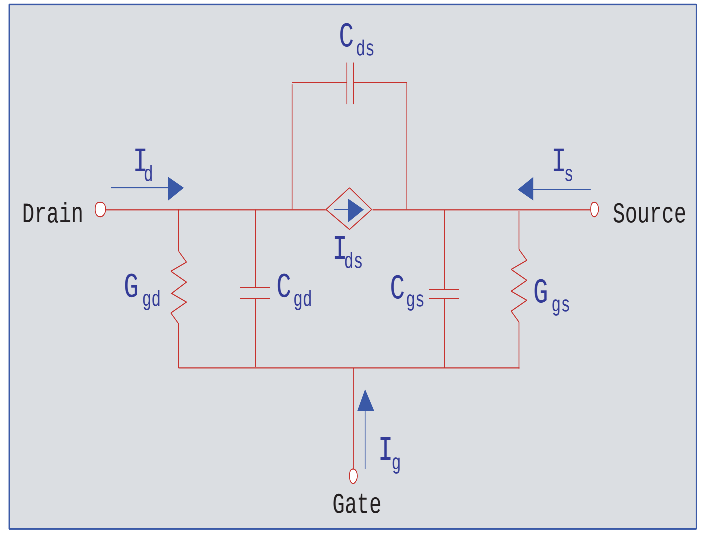

Fig. 1. Lumped Element Equivalent Circuit model for the NEC model 71000 FET.

where V_{dso} is the value of V_{ds} at which the coefficients A_0-A_3 are found and β is the coefficient for pinchoff change with V_{ds}. Following the example of reference [5], this paper uses the NEC 71000 series MESFET as a basis for all numerical examples. In order to apply this method to a typical FDTD/MRTD grid, an input voltage or current term is calculated for implementation in equation (3). In the circuit under consideration, input current terms are calculated at the gate and drain ports by taking a contour integral of the magnetic fields around the input line. As previously shown [7], the expanded stencil of the Battle-Lemarie scaling function allows for an accurate computation of this integral. This is due to the multi-cell nature of the scaling function. This property is discussed further in the Numerical Results section.

Once the input current is calculated, equation (3) is evaluated for the voltages at the gate and drain ports. The voltages are then related to electric fields by a line integration from the ground plane (or equivalent via) to the input line.

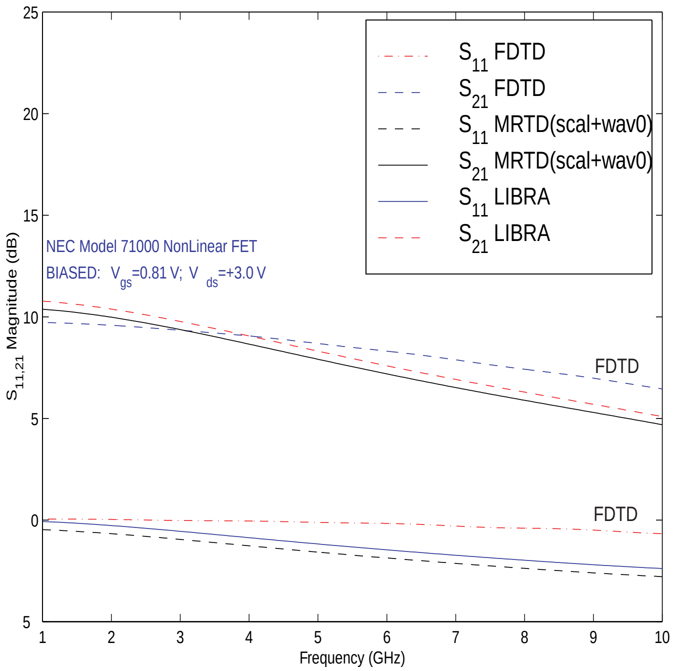

Fig. 2. Calculated S-parameters vs. frequency for the NEC71000 FET.

III. Numerical Results

The procedure described above is now applied to two separate cases. In the first case only a transistor is used between two lines in order to generate S-parameters for the circuit. In the second case, the generated S-parameters are used to design an amplifier matching network. In both cases results from MRTD are compared to those generated using LIBRA[8]. In the first case the method above is applied to the NEC Model 71000 MESFET connected to 50Ω microstrip lines at the gate and drain ports. Here, a dielectric substrate with $\epsilon_r = 2.33$ and a height of 20 mils is used, while the microstrip lines have a width of 60 mils. Additionally, the transistor is biased using DC sources, with $V_{gs} = -0.81V$ and $V_{ds} = +3.0V$.

Note that the input to the state equation are the currents calculated at the drain and gate ports, while the output to the difference equations are the voltages at the gate and drain ports. It is important to note that the input currents are found by calculating a path integral of the magnetic field terms at the gate/drain ports. Additionally, once the voltage terms are found, they are converted to electric fields thru a simple differential. As previously noted, it is expected that MRTD calculates these voltage and current terms more accurately than the FDTD method, due to the multi-cell nature of the MRTD scaling/wavelet functions. In Figure 2, comparisons between FDTD, MRTD and LIBRA are shown for the S-parameters of the transistor. In the MRTD simulations, both scaling functions and 0-order wavelet terms are applied to simulate the transistor. Good correlation is shown between MRTD and LIBRA, while the correlation between FDTD and LIBRA shows some discrepancies at higher frequencies.

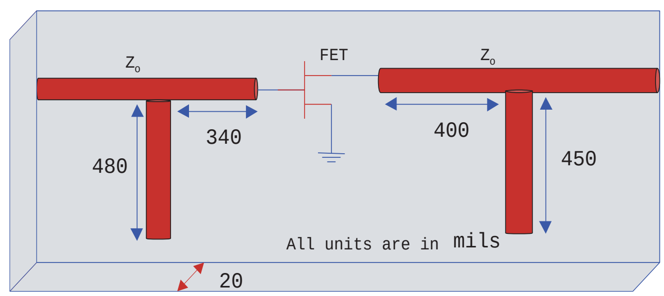

Fig. 3. Amplifier Circuit Setup.

In the second case, the S-parameters found above are used to design an amplifier matching network for specified gain of 14 dB at 6 GHz. Figure 3 shows a schematic of the amplifier matching network with lengths and dimensions of the stubs. Note that the microstrip parameters are the same as those used above. Here, it is important to consider the physical size of the transistor element. According to [9], the NEC71000 element is approximately 70 mils on a side. While the element size in this case does not affect the discretization of the microwave circuit, this will be a concern for smaller transistor elements.

Thus, it is possible to use only scaling functions to compute electric and magnetic fields in the dielectric and on the microstrip circuit elements. Then, using thresholding, calculate the input current and output voltage terms using scaling and 0-order wavelets, in order to ensure accuracy. Note that it is possible to use higher order wavelet terms if the circuit discretization warrants it. Consequently, wavelets can be used to distribute the nodes of the transistor over a much smaller cell. Calculated MRTD results are plotted in Figure 4 with respect to LIBRA. Once again, the two methods exhibit good correlation.

IV. Conclusions

In this paper, Multi-resolution Time Domain is applied to lumped element transistor devices using the equivalent source method. To validate the presented formulation, both a single transistor and an amplifier matching network are modeled. The S-parameters that result from this modeling are shown to compare well with commercial simulator results.

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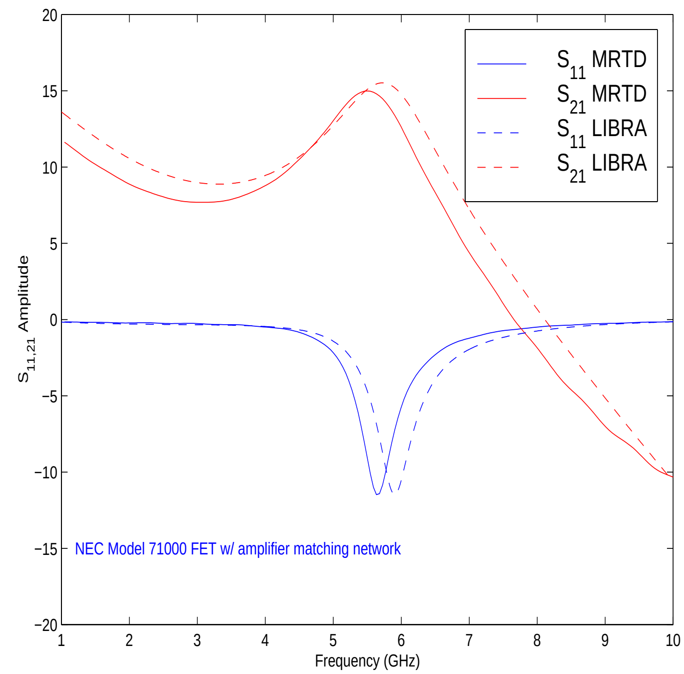

Fig. 4. Calculated S-parameters vs. frequency for amplifier matching network.